REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 19-38 are pending in the present application. Claim 27 is amended and Claim 38 is added by the present amendment.

In the outstanding Office Action, the specification was objected to; Claim 27 was objected to; and Claims 19-37 were rejected under 35 U.S.C. § 103(a) as unpatentable over Steely, Jr. et al. (U.S. Patent No. 6,088,771, herein "Steely") in view of Dieffenderfer et al. (U.S. Patent No. 5,822,608, herein "Dieffenderfer").

Regarding the objection to the specification, the specification has been amended as suggested by the outstanding Office Action and without adding new subject matter. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the objection to Claim 27, this claim has been amended as suggested by the outstanding Office Action. No new matter has been added. Accordingly, it is respectfully requested this objection be withdrawn.

The rejection of Claims 19-37 under 35 U.S.C. § 103(a) as unpatentable over Steely in view Dieffenderfer is respectfully traversed for the following reasons.

Briefly recapitulating, independent Claim 19 is directed to a state engine that receives multiple requests from a parallel processor for a shared state. The state engine includes at least one state element unit adapted to operate, atomically, on the

shared state in response to a request made by the parallel processor. Independent Claims 32, 35 and 36 recite features similar to independent Claim 19.

The claimed one state element unit advantageously achieves faster access for the parallel processor to the shared state, as shown for example in Figure 5(b) and its corresponding description in the specification.

Turning to the applied art, Steely discloses a technique that reduces a latency of a memory barrier operation used to impose an inter-reference order between sets of memory reference operations issued by a processor to a multiprocessor system having a shared memory. More specifically, Figure 1 shows a plurality of processors 112, 114, 116, and 118 connected via a switch 200 to a shared memory 150. Figure 2 shows that the switch 200 includes an arbiter 240 that arbitrates among input queues to grant access to the Arb bus 170, where the requests are ordered into a memory reference request stream. The arbiter 240 selects the request stored in the input queues for access to the bus in accordance with an arbitration policy, such as a conventional round-robin algorithm, as disclosed in Steely in the paragraph bridging columns 6 and 7.

Further, Steely discloses at column 7, lines 13-28, how a request Rd for data item "x" is received at the switch 200 from a processor P1 and loaded into an input queue 212. Then, the arbiter 240 selects the request in accordance with the arbitration algorithm discussed above and gains access to the ARB bus 170.

However, Applicant respectfully submits that it is known to the skilled in the art that an arbiter only controls or manages multiple accesses to a resource, usually a

memory as discussed above. The arbiter in Steely is provided simply to distinguish between accesses before and after a memory barrier event. Thus, the arbiter does not perform any function on the data as required by independent Claims 19, 32, 35, and 36.

On the contrary, the arbiter 240 of Steely simply controls the order in which the actions of the requesting processors are performed. In this respect, it is noted that the specification specifically discloses in the paragraph bridging pages 6 and 7 and the first three paragraphs on page 7 that a state element is provided with a function.

Therefore, Applicant respectfully submits that Steely is lacking not only the request made by the parallel processor, as acknowledged by the outstanding Office Action at page 4, third full paragraph, but also the state element being adapted to operate atomically on the shared state. In other words, the arbiter in Steely does not perform any function (does not operate) on the item of data, contrary to the state element of independent Claims 19, 32, 35, and 36.

Dieffenderfer has been considered but does not cure the deficiencies of Steely discussed above with regard to independent Claim 19. Further, Applicant respectfully submits that the claimed state engine operates on data in a fixed way or a plurality of fixed ways determined by a command word. On the contrary, Dieffenderfer discloses that the parallel processor has a stored program and performs conditional execution, which is different from the subject matter of independent Claims 19, 32, 35, and 36.

Accordingly, it is respectfully submitted that independent Claims 19, 32, 35, and 36 and each of the claims depending therefrom patentably distinguish over Steely and Dieffenderfer, either alone or in combination.

New independent Claim 38 has been added and finds support in the originally filed specification. More specifically, new independent Claim 38 finds support in pending Claims 19 and 25. No new matter has been added. As new Claim 38 includes the features of Claim 19, which is believed to be in condition for allowance as noted above, Applicant respectfully submits that new Claim 38 is also allowable.

All of the objections and rejections raised in the outstanding Office Action having been addressed, it is respectfully submitted that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, she or he is invited to contact the undersigned at (540) 361-2601.

Respectfully submitted,

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